Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently amended) A PLL circuit comprising:

a phase comparing means for comparing phases between a reference signal and an internal signal and outputting a phase difference signal according to a phase difference therebetween;

a plurality of oscillators which have mutually different frequency variable ranges and whose frequencies are respectively controlled in accordance with a phase ~~control~~difference signal;

a selecting means for selecting one of the outputs from the plurality of oscillators based on the phase difference signal~~ or the phase control signal~~; and

a frequency dividing means for generating the internal signal by dividing an oscillator output selected by the selecting means, wherein

provided is a means for approximating, when the oscillator selecting state is changed, an output phase of the frequency ~~divider~~dividing means to the phase of the reference signal.

2. (Original) The PLL circuit according to Claim 1, wherein

the plurality of oscillators have mutually overlapping frequency variable ranges.

3. (Currently amended) The PLL circuit according to Claim 1, wherein

the plurality of oscillators have mutually different operating ~~threshold voltage values~~frequency range.

4. (Currently amended) The PLL circuit according to ~~any one of Claims 1 through 3~~ Claim 1, wherein

the selecting means switches over outputs from the plurality of oscillators based on a history of the phase difference signal ~~or the phase control signal~~.

5. (Currently amended) The PLL circuit according to ~~any one of Claims 1 through 4~~ Claim 1, wherein

the oscillators are voltage controlled oscillators, and

provided is a means for converting the phase difference signal to ~~a~~an oscillator control voltage ~~value~~.

6. (Currently amended) The PLL circuit according to Claim 5, wherein

provided is a means for setting two threshold voltages having mutually different values within a variable voltage range of the ~~phase~~ control voltage of the voltage controlled oscillator and temporarily setting, when the voltage controlled oscillator selecting state is changed, a value of the ~~phase~~oscillator control voltage in a range between the two threshold voltages.

7. (Currently amended) The PLL circuit according to Claim 6, wherein

provided is a means for changing a value of the temporarily setting ~~phase~~oscillator control voltage in accordance with a history when the voltage controlled oscillator selecting state is changed.

8. (Currently amended) The PLL circuit according to Claim 6, wherein

when the voltage controlled oscillator selecting state is switched over as a result of the ~~phase~~oscillator control voltage becoming out of the range between the two threshold voltages, the temporarily setting phase control voltage is set, out of the two threshold voltages, in the vicinity of the ~~phase~~oscillator control voltage-side threshold voltage.

9. (Currently amended) The PLL circuit according to Claim 6, wherein

when the voltage controlled oscillator selecting state is switched over as a result of the ~~phase~~oscillator control voltage becoming out of the range between the two threshold voltages and when the ~~phase~~oscillator control voltage becomes out of the range between the two threshold voltages twice or more in series, the temporarily setting ~~phase~~oscillator control voltage is set, out of the two threshold voltages, in the vicinity of the ~~phase~~oscillator control voltage-side threshold voltage.

10. (Currently amended) The PLL circuit according to Claim 6, wherein

when the ~~phase~~oscillator control voltage becomes out of the range between the two threshold voltages, depending on whether this ~~phase~~oscillator control voltage is higher than the two threshold voltages or lower than the two threshold voltages, whether setting the ~~phase~~oscillator control voltage higher or setting the same lower than an intermediate potential between the two threshold voltages is controlled.

11. (Currently amended) A PLL circuit comprising:

a phase comparing means for comparing phases between a reference signal and an internal signal and outputting a phase difference signal according to a phase difference therebetween;

a plurality of resonant circuits provided with mutually different resonance frequencies;

an oscillator whose oscillation frequency is controlled in accordance with the resonant circuits and a phase ~~control~~difference signal;

a selecting means for selecting one of the plurality of resonant circuits based on the phase difference signal ~~or the phase control signal~~; and

a frequency dividing means for generating the internal signal by dividing an output from the oscillator, wherein

provided is a means for approximating, when the resonant circuit selecting state is changed, an output phase of the frequency ~~divider~~dividing means to the phase of the reference signal.

12. (Currently amended) The PLL circuit according to Claim 11, wherein

the selecting means switches over the plurality of resonant circuits based on a history of the phase difference signal ~~or the phase control signal~~.

13. (Currently amended) The PLL circuit according to Claim 11 ~~or 12~~, wherein

the oscillator is a voltage controlled oscillator, and

provided is a means for converting the phase difference signal to ~~a~~an oscillator control voltage ~~value~~.

14. (Currently amended) The PLL circuit according to Claim 13, wherein

provided is a means for setting two threshold voltages having mutually different values within a variable voltage range of the ~~phase~~ control voltage of the voltage controlled oscillator and temporarily setting, when the resonant circuit selecting state is changed, a value of the ~~phase~~oscillator control voltage in a range between the two threshold voltages.

15. (Currently amended) The PLL circuit according to Claim 14, wherein

provided is a means for changing a value of the temporarily setting ~~phase~~oscillator control voltage in accordance with a history when the resonant circuit selecting state is changed.

16. (Currently amended) The PLL circuit according to Claim 14, wherein

when the resonant circuit selecting state is switched over as a result of the ~~phase~~oscillator control voltage becoming out of the range between the two threshold voltages, the temporarily setting ~~phase~~oscillator control voltage is set, out of the two threshold voltages, in the vicinity of the ~~phase~~oscillator control voltage-side threshold voltage.

17. (Currently amended) The PLL circuit according to Claim 14, wherein

when the resonant circuit selecting state is switched over as a result of the ~~phase~~oscillator control voltage becoming out of the range between the two threshold voltages and when the ~~phase~~oscillator control voltage becomes out of the range between the two threshold voltages twice or more in series, the temporarily setting ~~phase~~oscillator control voltage is set, out of the two threshold voltages, in the vicinity of the ~~phase~~oscillator control voltage-side threshold voltage.

18. (Currently amended) The PLL circuit according to Claim 14, wherein

when the ~~phase~~oscillator control voltage becomes out of the range sandwiched between the two threshold voltages, depending on whether this ~~phase~~oscillator control voltage is greater than the two threshold voltages or smaller than the two threshold voltages, whether setting the ~~phase~~oscillator control voltage higher or setting the same lower than an intermediate potential between the two threshold voltages is controlled.

19. (Currently amended) A PLL circuit comprising:

a phase comparing means for comparing phases between a reference signal and an internal signal and outputting a phase difference signal according to a phase difference therebetween;

an oscillator constructed by coupling a plurality of delay circuits whose delay times are respectively controlled in accordance with a phase ~~control~~difference signal;

a selecting means for switching over the coupling number of delay circuits based on the phase difference signal ~~or the phase control signal~~; and

a frequency dividing means for generating the internal signal by dividing an oscillator output selected by the selecting means, wherein

provided is a means for approximating, when the oscillator selecting state is changed, an output phase of the frequency ~~divider~~dividing means to the phase of the reference signal.

20. (Currently amended) The PLL circuit according to Claim 19, wherein

the selecting means switches over the coupling number of the delay circuits based on a history of the phase difference signal ~~or the phase control signal~~.

21. (Currently amended) The PLL circuit according to Claim 19 ~~or 20~~, wherein

the oscillator is a voltage controlled oscillator, and

provided is a means for converting the phase difference signal to ~~a~~an oscillator control voltage ~~value~~.

22. (Currently amended) The PLL circuit according to Claim 21, wherein

provided is a means for setting two threshold voltages having mutually different values within a variable voltage range of the ~~phase~~ control voltage of the voltage controlled oscillator and temporarily setting, when the delay circuit coupling number selecting state is changed, a value of the ~~phase~~oscillator control voltage in a range between the two threshold voltages.

23. (Currently amended) The PLL circuit according to Claim 22, wherein

provided is a means for changing a value of the temporarily setting ~~phase~~oscillator control voltage in accordance with a history when the delay circuit coupling number selecting state is changed.

24. (Currently amended) The PLL circuit according to Claim 22, wherein

when the delay circuit coupling number selecting state is switched over as a result of the ~~phase~~oscillator control voltage becoming out of the range between the two threshold voltages, the temporarily setting ~~phase~~oscillator control voltage is set, out of the two threshold voltages, in the vicinity of the ~~phase~~oscillator control voltage-side threshold voltage.

25. (Currently amended) The PLL circuit according to Claim 22, wherein

when the delay circuit coupling number selecting state is switched over as a result of the ~~phase~~oscillator control voltage becoming out of the range between the two threshold voltages and when the ~~phase~~oscillator control voltage becomes out of the range between the two threshold voltages twice or more in series, the temporarily setting ~~phase~~oscillator control voltage is set, out of the two threshold voltages, in the vicinity of the ~~phase~~oscillator control voltage-side threshold voltage.

26. (Currently amended) The PLL circuit according to Claim 22, wherein

when the ~~phase~~oscillator control voltage becomes out of the range between the two threshold voltages, depending on whether this ~~phase~~oscillator control voltage is greater than the two threshold voltages or smaller than the two threshold voltages, whether setting the ~~phase~~oscillator control voltage higher or setting the same lower than an intermediate potential between the two threshold voltages is controlled.

27. (Currently amended) The PLL circuit according to ~~any one of Claims 1 through 26~~ Claim 1, wherein

the output phase of the frequency dividing means is synchronized with the phase of the reference signal.